Investigation of Thermal Performance of Various Power-Device Packages

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Abstract

Continuing trends of miniaturization, rising switching frequencies and increasing packaging densities require increased current handling capability of packaged devices in applications related to power conversion. Traditionally, these ever-increasing demands are met by improvements in silicon efficiency. Nevertheless, with silicon efficiency pushed to the limit, major semiconductor power-device manufacturers are now looking for innovative packaging options for power devices to achieve the next level of breakthroughs in electrical and thermal performance. This paper presents a comprehensive study of thermal behaviors of various power-device packages. CFD-based FLOTHERM has been applied to calculate the junction-to-ambient thermal resistance with the industry standard-specified board attachment. Fundamental cooling mechanisms associated with different packaging technologies, including wire-bond, strap bonding, flip chip and ball grid array (BGA), and wafer-level packaging are investigated. The impact of internal package design on the thermal performance of various packages is discussed in detail. A thermal analysis of multichip module for leadless and BGA technologies is also presented.

Introduction

Applications demanding high-power conversion such as voltage regulator module for microprocessors, automotive electronics and telecommunications, have introduced a trend for achieving higher power densities at lower cost [1,2]. Over the past decades, this trend has been successfully met by increasing silicon efficiency; however, future requirements dictate further improvement in overall system efficiency, which can only be achieved through innovations in packaging [3-5]. Accordingly, in recent years, semiconductor industry has taken aggressive steps towards achieving small form factor power packages with significant improvements in electrical and thermal performance. From traditional plastic injection-molded and wire-bonded package, power packaging has come a long way where state of the art IC packaging techniques such as ball-grid-array, chip-scale packaging and leadless, and wafer-level packaging are being used [6-9].

Leaded packages such as TO-220s and axial leaded devices had been the packaging configurations of power devices for the longest time. However, as miniaturization and functional integration became the dominant drivers for electronics components and modules, new technologies emerged[2]. The DPAK package was introduced first in mid-1980, which caused a major paradigm shift in the package design arena. At the same time, an alternative package with SOT-223 came along, which offered smaller outline than DPAK yet used the footprint and pin-outs. Then came D2PAK in the early 1990s, which offered usage of bigger die size in a package, thus increasing current handling capability significantly and reducing thermal resistance of the package to some extent. The SO-8 packages were introduced in the mid-1990, which allowed significant size reduction compared to DPAK packages and resulted in fewer packages required for assembly while reducing board space. This improvement was made possible since the die size reduction and more cells per inch of silicon enabled designers to achieve the same type of RDS(on) performance in SO-8, which was previously only available in TO-220 and DPAK configurations [8].

However, continued miniaturization drive demanded even smaller and more efficient package than SO-8 packages to meet future thermal and electrical requirements. This new surge of design revolution has two specific market demands – higher current requirements in microprocessors and low RDS(on) in a smaller area for power management. Accordingly, a new stream of packaging configurations emerged for packaging discrete power devices as well as multi-chip modules since the beginning of 2000 [7]. Figure 1 presents a snapshot of the evolution of power-device packaging from the leadframe based to flip chip and ball grid array technologies.

Liu et al [10, 11] introduces the general methodology of the simulation interface and platform. This simulation tool has been applied to MLP package family. The results agree well with those from the classic ANSYS and measurement. Tounsi et al. [12] developed specific thermal simulation tools to perform electro-thermal simulation of power devices or circuits. 3D and transient flow spreading effects in multilayered substrates commonly used in power component packaging as well as in hybrid power circuits were considered. Kasem [13] investigated the influence of the design and physical limitations on the performance of thin quad flat packages

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(TQFPs) b using a 3-D finite element scheme. A methodology for low profile 48-lead TQFPs was outlined. Ganesa-Pillai and Chen [14] presented a finite-element thermal analysis of a boost converter module, which integrated all the semiconductor devices and the snubber circuits of a boost converter on a ceramic substrate. The effects of different substrates and use of multiple current sharing components were examined. Katsis and Van Wyk [15] compared the thermal impedance of modules with varying void area at a constant power dissipation level in order to develop a relationship between thermal impedance and void area. The effect of aging on thermal transient behavior was correlated to finite element thermal simulations. Chiriac and Lee [16] performed a detailed thermal analysis for the wirebonded GaAs devices by using numerical simulations. The main focus was on the impact of die attach thermal conductivity, substrate's top metal layer thickness, and via wall thickness on the overall thermal performance of GaAs IC device . Arik Garg, and Bar-Cohen [17] explored the thermal challenges in advanced system-on-package (SOP) electronic structures, as well as candidate thermal solutions for these highly demanding cooling needs. Detailed three-dimensional (3-D) finite-element simulations were used to study the temperature distributions in a typical SOP package, and to provide guidance for the development and implementation of "compact thermal models". Direct liquid cooling by immersion of the components in inert, nontoxic, high dielectric strength perfluorocarbon liquids was seen effective over a range of anticipated SOP power dissipations. Chiriac and Lee [18] performed a detailed numerical study to examine the thermal characteristics of a chip set at the system level. The chip set included the Power Amplifier (PA) module, power management and base-band packages, front-end receiver package and memory. Detailed solid modeling was applied to the PA module with the GaAs (Gallium Arsenide) device bonded to a multi-layer ceramic substrate. Frank [19] discussed two methods of defining the thermal junction-ambient resistance and the commonly used wave solder assembly technology. The test setup and the results of tests done with various packages and transistors were also described. Kandasamy and Subramanyam [20] numerically evaluated the performance of the package different die sizes and apoxy molding compounds at different power levels. The use of heat slug was investigated to identify its effect on heat dissipation for IC generation.

In this paper, a comprehensive study to investigate thermal behaviors of various types of power-device packages was presented. The packages under investigation include traditional DPAK, D^{2}PAK, leadless package, SO, flip chip, BGA, and wafer-lever CSP packages. We have analyzed the motivations for small form factor packaging of power devices from a power conversion point of view. Current and future design requirements of voltage regulator modules for microprocessors are also analyzed. The extensive thermal simulations have been performed to understand the thermal limitations with regard to each technology and the possible options to improve the thermal performance.

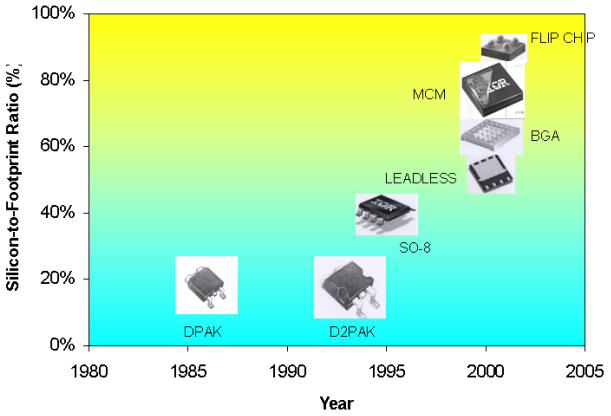


Fig. 1 Evolution of discrete and multi-chip packaging configurations of power devices

Background

The junction temperature of power device depends on many factors, including the packaging design (interconnect and structure), board selection (material, structure and interface), heat sink attachment (heat sink design and interface materials), ambient conditions (ambient temperature and air flow speed), as well as the system integration. The package design plays a very important role in overall thermal management because it provides the first 'gate' for the heat dissipation from the silicon chips. The demands of the continuing miniaturization of the system with maximized thermal performance require innovative package designs.

The thermal resistance is defined as

$$R = \frac{T_{j,\max} - T_{\text{ref}}}{P} \qquad (1)$$

where $T_{j,\max}$ is the maximum junction temperature, T_{ref} is the reference temperature and P is the power dissipation of the package. There are different selections of the reference temperature, such as following:

$R_{j\text{-}a}$: junction-to-ambient thermal resistance, where T_{ref} is taken as the ambient temperature;

$R_{j\text{-}c}$: junction-to-case thermal resistance, where T_{ref} is taken as the maximum case temperature on the top of the package;

$R_{j\text{-}b}$: junction-to-board thermal resistance, where T_{ref} is taken as the maximum board temperature that the package is attached to;

$R_{j\text{-}l}$: junction-to-lead thermal resistance, where T_{ref} is taken as the lead package for leaded packages.

Thermal resistance such as $R_{j\text{-}c}$, $R_{j\text{-}b}$, or $R_{j\text{-}l}$ is a local measure for the thermal performance in a particular heat dissipation path. For example, $R_{j\text{-}b}$ represents the thermal resistance between the junction and the board only and therefore, does not fully represent the thermal performance of the overall package. Therefore, in our investigations, the thermal resistance of a package is

defined as the junction-to-ambient thermal resistance in steady-state, i.e., $R_{j\text{-}a}$.

Unless otherwise stated, the package is mounted on 1 in^2 of 2 oz copper on FR4 in our following investigations according to the industry standards. The ambient temperature (temperature in chassis) is assumed to be 50°C under the natural convection condition. The effects of the ambient temperature and the air speed (forced convection) on the thermal resistance are also briefly addressed. The FLOTHERM simulation tool has been used for the analysis.

Modeling

For the leadframe-based packages, the lead fingers are modeled discretely for DPAK, D^2PAK, and SO-8 packages. When the leadframe has a great number of leads, the detailed modeling will lead to the huge amount of grid cells in the numerical analysis. Therefore, a lumped cuboid with an orthotropic (i.e., directionally dependent) conductivity is used. This means that the conductivity in the direction along the leads would be obtained by an assumption of parallel resistance, whereas the conductivity in the transverse direction would be obtained by an assumption of series resistance. This would avoid spurious spreading of the lumped leadframe cuboid in the transverse direction in the model. The results show that the lumped model presents an excellent agreement (1% difference in junction temperature) with detailed model. For the flip-chip/BGA packages, the solder balls are lumped and replaced by an equivalent volume of same material. The gaps between the solder balls, when underfill is not applied, are filled with air. Considering that the thickness of gaps is rather small (~ 100μm), the air inside is almost in still state, and is modeled in conduction mode.

Most of studies do not consider the impact of radiation effect. This may be true in forced convection condition, in which convection becomes dominant in heat dissipation. However, under the natural convection condition, the radiation effect may be comparable to the convection. In Fig. 2, the differences of thermal resistance due to the radiation effect are shown for a DPAK package.

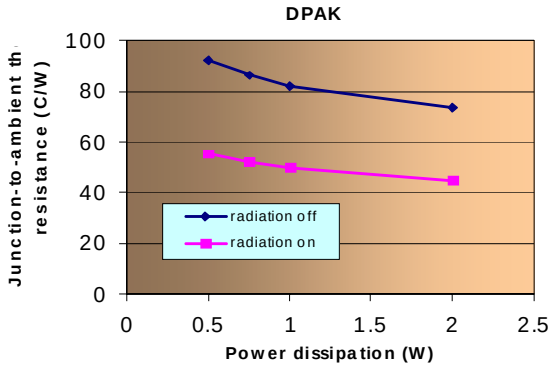


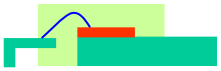
Fig. 2 Radiation effect on thermal resistance for DPAK packages in natural convection

Radiation effects play a very significant role in heat dissipation under natural convection. Almost 50% of heat is dissipated through the radiation. This suggests that in thermal modeling of a package under natural convection, the radiation effect must be turned on. Therefore, all the thermal models developed in this paper will consider the radiation effect.

DPAK and D^2PAK Packages

DPAK or D^2PAK packaged power devices have excellent current handling and thermal dissipation capabilities. Table 1 lists the typical dimensions of the DPAK and D2PAK packages, respectively. The package dimension in the table refers to the foot-print-area. It can be seen that D^2PAK is almost twice as large as DPAK in terms of die area and package thickness

Table 1 Dimensions of DPAK and D^2PAK (unit: mm)



A DPAK or D^2PAK

	DPAK	*D^2PAK*
Die	**2.6x3.9**	**4.0x5.6**
Package	**9x6.5**	**12.8x10**
Profile	**2.3**	**4.5**

Fig. 3 plots the thermal resistance as function of power dissipation for DPAK and D^2PAK respectively. The differences in thermal resistance are not significant (less than 5°C/W), in spite of obvious differences in physical sizes between DPAK and D^2PAK. This is primarily because the package is mounted on 1 in^2 of 2 oz copper on FR4. The uniformly-distributed copper on the top of FR4 makes the board highly thermal conductive. As an extreme opposite situation where the package is mounted onto 1 in^2 of bare FR4 only with 0.3 W/m^2K thermal conductivity, Table 2 list the results of the thermal resistance for both DPAK and D^2PAK packages. It clearly shows that the board material has significant influence on the package thermal performance. This means that the better thermal performance may be achieved even with smaller packages by effective board design. Nevertheless, without loss of generality, in our following studies all thermal resistance data refer to the 2 oz copper on FR4 according to the standards. This makes it easier to compare the simulated data with the published data.

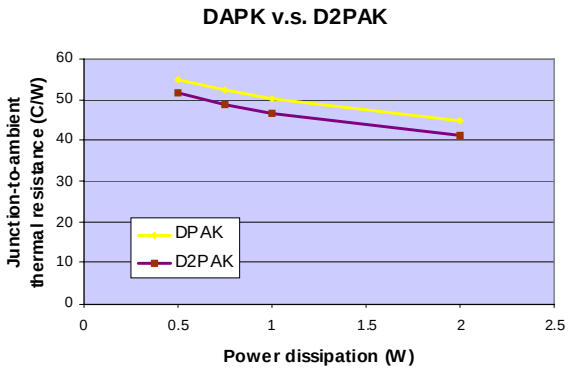


Fig. 3 Thermal resistance as function of power dissipation for DPAK and D^{2}PAK packages

Table 2 Thermal Resistance of DPAK and D^{2}PAK Packages

	DPAK	*D^{2}PAK*
Bare FR4	**186.6**	**104.5**
2oz copper on FR4	**50.2**	**46.6**

Standard Outline (SO) Packages

The original standard IC SO-8 package uses wires on the top of chip to connect all leads (see. Fig.4a). The standard power MOSFET SO-8 package uses wires to connect the source and gate to the leads, but for the drain sides, the leads are directly connected with the die pad, as shown in Fig. 4b. Thermal behaviors between these two packages can be very different, which will be discussed later. In order to improve the thermal and electrical performance of SO-8 packages, a solid copper strap that covers the surface of the die is adopted to replace the wirebonds connecting source to the leadframe (Fig. 4c). This provides highly conductive path in addition to the existing path through the die pad connected to the leads.

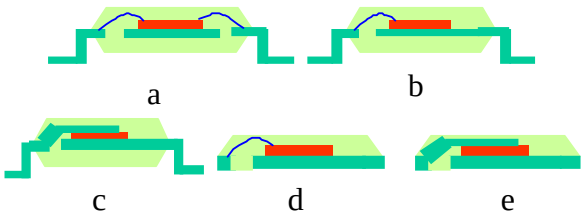


Fig. 4 Various types of SO-8 packages a: standard IC; b: standard power MOSFET; c: strap-bonded; d: leadless; e: strap-bonded with leadless

Thermal performance can be further improved by providing a direct path from the backside of the copper die attach pad to the board (Fig. 4d). The main thermal path is through the large copper pad exposed on the bottom of the package, which would improve thermal resistance dramatically. This package is usually called leadless package or micro-leadframe package.

Fig. 5 plots the thermal resistance of different types of SO-8 packages with same die size and package dimension. We notice a huge difference in thermal resistance between the standard IC SO-8 and standard power MOSFET SO-8. The direct connection of copper die pad to the leads in standard power MOSFET SO-8 provides a path for heat dissipation to reduce the junction temperature dramatically. Reduction of thermal resistance by using strap bonding is about 15.2% over the standard power SO-8 package, as shown in Fig.5. When the leadless package format is adopted, the thermal resistance can be reduced to 52°C/W, comparable to the thermal resistance of DPAK packages, but with much smaller package dimensions and lower profile. The thickness of DPAK and leadless packages are 2.3 mm and 1.1 mm, respectively. Fig. 5 suggests that even though the package dimension and chip size remain unchanged, thermal performance can be significantly improved by an appropriate package design and improved interconnect. For example, with an ambient temperature of 50°C and 1 Watt power dissipation for the chip, the junction temperature with standard IC SO-8 package is as high as 201.8°C. However, with leadless package, the junction temperature drops to 102.3°C.

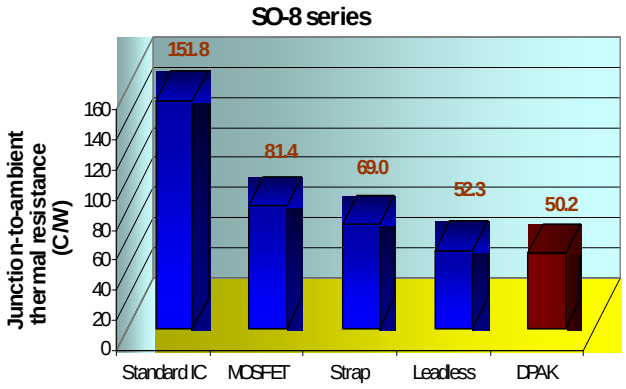


Fig. 5 Comparison of thermal resistance for various SO-8 packages

The question remains if any further thermal benefit could be gained with the strap bonding applied to a SO-8 leadless package, as shown in Fig. 4e. Fig. 6 plots the simulation results compared to other types of power SO-8 packages. The improvement is almost negligible in comparison to leadless packages from a thermal point of view. The heat dissipation by the direct contact of copper pad to the board in leadless package is so dominant that heat dissipation through strap bonding is minimal.

Fig. 5 and Fig. 6 present a clear picture how the package design affects the thermal behaviors. We notice that in Fig. 4, three of these packages, i.e., standard power SO-8, strap bonded, and leadless packages, have applications in power electronics. However, the comparisons of these packages to the standard IC SO-8 and strap boned leadless packages, reveal the fundamental cooling mechanism associated with the package design. The package thermal performance can be enhanced by providing a direct path for the heat dissipation between chip and board. When a package is designed such as

leadless, in which the heat dissipation is maximized in one path, the improvement by additional heat path would be insignificant.

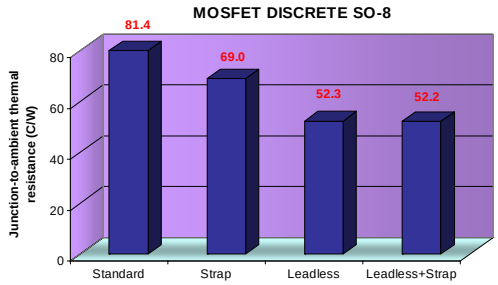


Fig.6 Comparison of strap bonding applied to leadless SO-8 with other types of SO-8 packages

Flip Chip (FC)/Ball Grid Array (BGA) Packages

Flip-chip-on-board or wafer-level power package uses the chip-scale packaging technology to bring all of the terminals on a single side of the die (see Fig. 7). Since the die itself is the package, a flip chip on board package has a nearly 100% silicon-to-footprint ratio. The main heat dissipation path will be the solder balls and underfill (if any). Although the chip is directly attached to the board through the solder balls, which gives the direct path of heat dissipation, questions remain how the solder ball geometry, layout and number of solder balls would affect the thermal performance. Would it be necessary to use the underfill from a thermal point of view? In order to address these questions, thermal models are developed here with chip size same as that used for SO-8 package. A single solder ball diameter is assumed to be 250μm and the pitch between the solder balls is 800μm. Three cases for solder ball layouts, 2x2, 3x4, and 4x5 arrays, are considered, as shown in Fig. 7.

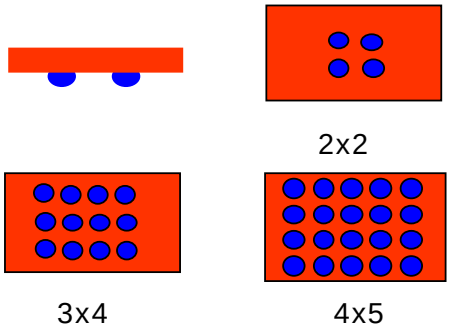


Fig. 7 Flip chip on board packages with different numbers of solder balls

In Fig. 8 the thermal resistance is shown for a flip-chip-on-board package with different combinations of solder balls when underfill is not applied. The thermal resistance results in the presence of underfill are given in Fig. 9. The results have shown that underfill has major contributions to the thermal dissipation despite of its relative low thermal conductivity (~ 0.9 W/Km).

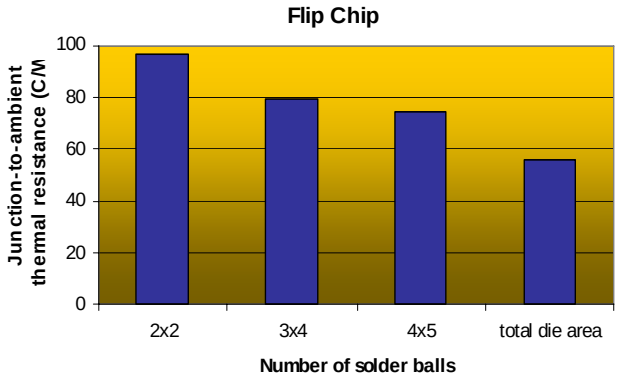


Fig. 8 Thermal resistance of a flip-chip-on-board package with different numbers of solder balls

When underfill is applied, the number of solder ball on thermal resistance has insignificant effect. However, in the absence of underfill, thermal resistance can be significantly reduced with increasing of the number of solder balls. As an extreme case, where the entire contact area between board and chip is solder contact, Fig. 8 shows that the minimum thermal resistance for this package is about 55.7°C/W. The difference between the extreme case and the case with 2x2 solder balls with underfill is not significant. These results imply that in flip chip applications, underfill is necessary to improve both thermal and reliability performances. The number of solder balls with underfill virtually gives no significant influence on thermal behaviors.

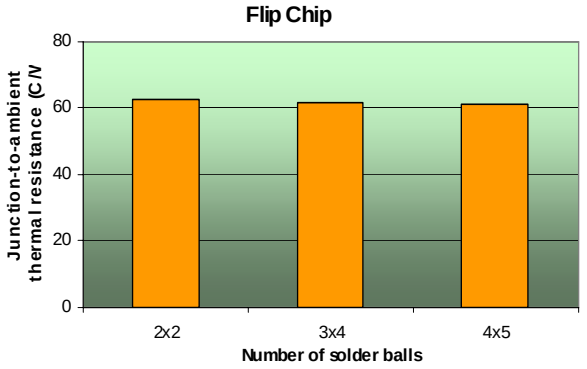


Fig. 9 Thermal behaviors of flip chip on board packages with underfill

Another version of flip chip application in power devices is the ball grid array package shown in Fig. 10a. The drain side is connected to the solder ball through the conduction layer, which is encapsulated by the epoxy-based materials. In this package the die size is same as flip chip on board package. A full array of solder balls with 6x5 is assumed over the package. The heat can be dissipated through the solder balls directly beneath the chip and those connected to the drain side. Fig. 11 investigates the effect of the conduction layer on the thermal dissipation. It is interesting to note that, unlike the strap bonds used in SO-8 packages (Fig. 4c), where the copper strap improves thermal performance significantly,

the conduction layer (copper) used in BGA as shown in Fig. 10 has negligible effect on thermal resistance. "No conduction layer" in Fig. 11 means that the conduction layer has very low thermal conductivity (~ 0.9 W/Km) which, of course, is not realistic. The results imply that the heat dissipation is dominant through the path of solder balls under the chip. Fig. 11 also shows the effect of underfill on thermal resistance. The improvement is about 12% reduction over the same package without underfill.

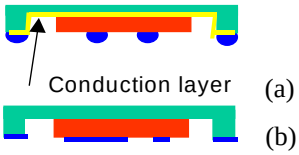


Fig. 10 a): ball grid array (BGA) MOSFET package; b): large contact interconnect MOSFET package

A ball grid array approach, even with multiple balls per connection has a limited contact area with a printed circuit board and hence the thermal performance junction to board and conduction efficiency cannot be maximized. Therefore an underfill material is required in the above applications. An alternate interconnection methodology that addresses this issue has been developed using a large area solder-contact technique. Fig. 12 presents the results of thermal resistance for large contact interconnect compared to the BGA package discussed before. We notice a 10% reduction in thermal resistance over the BGA package.

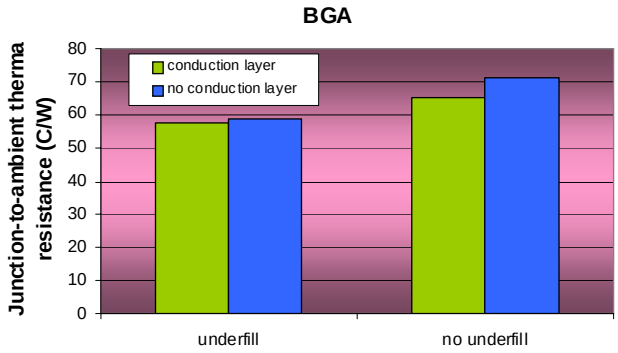


Fig. 11 Thermal resistance of full array BGA MOSFET packages

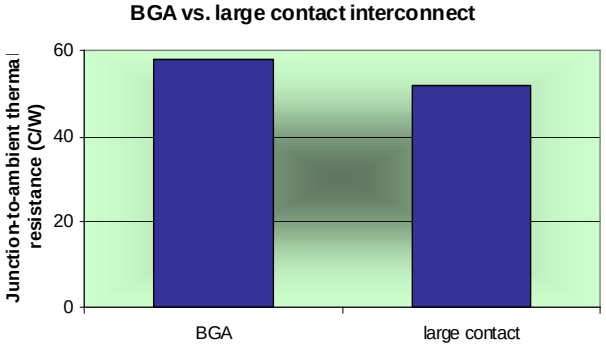


Fig. 12 Comparison of thermal resistance between BGA and large contact area power device package

Multichip Module (MCM)

A multichip module, which contains a control IC and two power MOSFETs was studied. The leadless package technology was selected and the package profile is below 1mm. A similar module with a ball grid array (BGA) is also studied, as shown in Fig. 13. Two MOSFETs and an IC chip are assumed to dissipate power 0.4, 0.4 and 0.2 Watt, respectively. Fig. 14 shows that leadless (so-called 'PIP') has better thermal performance, with 16.9% lower thermal resistance, than 'BGA'. In Fig.15 the maximum junction temperatures for each chip in the module are given for both packages under steady-state condition. The difference of the junction temperature in different chips is very small in spite of the non-uniformity in power dissipation.

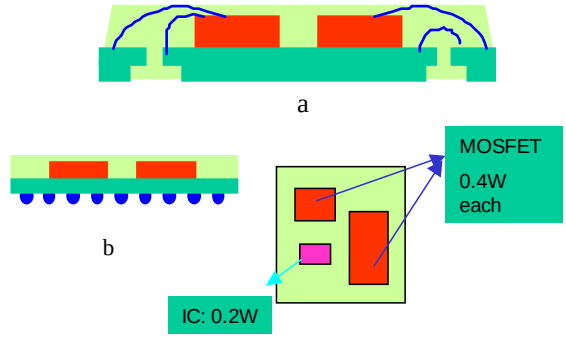


Fig. 13 Multichip module: a: PIP; b: BGA

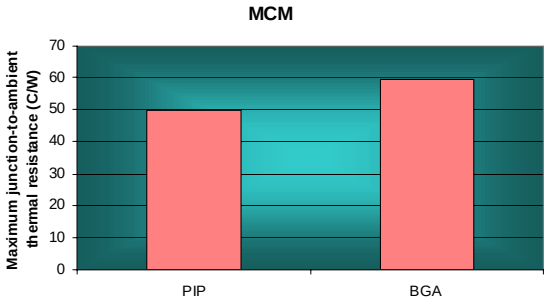


Fig. 14 Comparison of thermal performance between 'PIP' and 'BGA' of multichip module

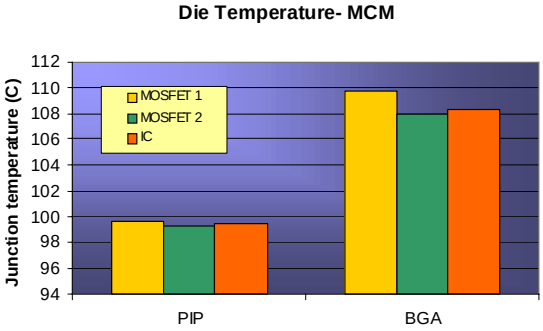


Fig. 15 junction temperature for each chip in MCM

Conclusions

Thermal models have been developed for various power-device packages. The CFD-based FLOTHERM simulation tool has been applied to predict the junction-to-air thermal resistance of different packages. It has been found that the difference in thermal resistance between DPAK and D2PAK under the same power dissipation is not significant (less than 5°C/W), in spite of the large differences in die size and package dimensions. This is primary because the package is mounted onto 2oz copper on FR4, which makes the board highly thermal conductive. Due to the large contact area between the copper pad and board, DPAK package displays the least thermal resistance (~50°C/W) and thus sets a baseline to evaluate other types of packages.

SO-8 power packages present a wide range of thermal resistance (50-80°C/W) when different interconnect technology and package format are applied. Strap bonding can improve thermal performance about 15% over the traditional SO-8 power MOSFET. The leadless or micro leadframe package further reduces the thermal resistance to the level comparable to the DPAK, with smaller package dimensions.

Flip-chip-on-board packages or ball grid array (BGA) packages have relatively good thermal performance (50-70°C/W) due to the direct solder interconnect to the board. When underfill is applied, the size and number of solder balls do not matter. However, the thermal performance has strong dependence on the number of solder balls if underfill is not used. The large area contact technology developed maximizes the thermal performance of the flip chip packages to the level of traditional DPAK.

For multichip modules, leadless module achieves better thermal performance (16.9% reduction of thermal resistance) than a similar module using BGA version.

A superior advantage of flip chip packages over wire-bonded packages is the realization of double-sided cooling mechanism. When a heat sink is attached, the thermal behaviors may be completely different from the behaviors shown above. Care must be taken to use the above results in an actual system application either from the predicted thermal resistance or the data from the data sheets, because thermal resistance depends not only on the package design and interconnect, but also on the ambient conditions, heat sink attachment and the board selection.

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